REMARKS

Claims 1-20 are presented for further examination. Claims 1, 3, 4, 5, 9, 14, 15, 18, and 19 have been amended. Claims 21 and 22 are new.

In the Office Action mailed November 30, 2005, the Examiner objected to the abstract because of excessive length. Claim 1 was objected to because of grammatical informalities, and claim 4 was rejected under 35 U.S.C. § 112, second paragraph, for lack of antecedent basis of "said state maintaining means." Claims 1-9, 12, 13, and 18-20 were rejected under 35 U.S.C. § 102(b) as anticipated by U.S. Patent No. 5,699,530 ("Rust et al."). Claims 10, 11, and 14-17 were rejected under 35 U.S.C. § 103(a) as unpatentable over Rust et al. in view of U.S. Patent Publication No. 2002/0199042 ("Kim et al.").

Applicants respectfully disagree with the bases for the rejections and request reconsideration and further examination of the claims.

Abstract of the Disclosure

Applicants are submitting herewith a rewritten Abstract of the Disclosure that is within the 150-word limitation. No new matter has been added. Approval and entry of the Abstract is respectfully requested.

Objections and § 112 Rejection

Claim 1 has been amended so that the two phrases "read pointer generating" appearing at lines 8, 10, and 16 now "read pointer-generating" as the Examiner requested. Claim 3 has similarly been amended. Claim 4 has been amended to remove the recitation of "said state maintaining means" at line 1 and "state controlling means" has been substituted therefore.

Rejection on the Merits

Claim 1 is directed to a FIFO buffer that provides reduced access times without introducing any latency overhead. The buffer includes FIFO means, read data selection means connected to data output terminals of the FIFO means and having two data output terminals

providing simultaneous access to a selected storage location, odd and even read pointer-generating means, multiplexing means coupled to each of the two data output terminals of the read data selection means for selecting one of the outputs from the read data selection means, and state controlling means coupled to the multiplexing means for controlling the selection of the final FIFO output and to the odd and even read pointer-generating means.

The Examiner has applied Rust et al. (U.S. Patent No. 5,699,530) as teaching all of the elements of the claimed invention. Applicants respectfully disagree. Figure 4 of Rust et al. shows an even array and an odd array of FIFO memory, each having a single output coupled to a multiplexer 118. A write pointer matrix and read pointer matrix are also provided for addressing the even and odd arrays. These matrices are also coupled to the multiplexer 118.

What Rust et al. do not show are the claimed read data selection means and the state controlling means. More particularly, as shown in Figure 3 of the present application, the FIFO (301) has the plurality of outputs coupled to a data select circuit (303) that in turn has two outputs coupled to a multiplexer (306). Nowhere do Rust et al. teach or suggest the claimed read data selection means between the multiplexer (118) and the even and odd arrays (102), (104) as recited in claim 1 of the present invention.

Figure 3 of the present invention also shows a finite state machine (310) having outputs coupled to the multiplexer (306) and to the odd and even read pointer-generating circuits (304), (305). Nowhere do Rust et al. teach or suggest the use of such a finite state machine as recited in claim 1.

On pages 4-5 of the remarks accompanying the first Office Action, the Examiner asserts that Rust et al.'s multiplexer 118 is a read data selection means. However, the multiplexer 118 of Rust et al., even if it could be considered a read data selection means, does not have the claimed two data output terminals. Rather, the multiplexer 118 of Rust et al. has only a single output as shown in Figure 4.

The Examiner is also asserting that the multiplexing means recited in claim 1 is met by the multiplexer 118 of Rust et al. However, the multiplexer 118 of Rust et al. cannot be both the read data selection means and the multiplexing means of claim 1. This inconsistency is evident from the last paragraph on page 4 if the Office Action where the Examiner identifies the

multiplexing means as coupled to two data output terminals (elements 112 and 114) of the read data selection means. If the multiplexer 118 is functioning as the claimed multiplexer, then it cannot have two data output terminals.

In view of the foregoing, it is clear that Rust et al. do not teach all of the elements and features of claim 1. Applicants respectfully submit that claim 1 is clearly allowable over Rust et al. Dependent claims 2-4 are also allowable for the features recited therein as well as for the reasons why claim 1 is allowable. For example, claim 2 recites a FIFO status providing means, which is shown in Figure 3 in part as element FIFO status (309). In remarks accompanying the rejection on page 5, paragraph 8, the Examiner asserts that Rust et al. teach buffers and methods that comprise FIFO status providing means coupled to a selected read pointer means for generating FIFO status signals ("signals from elements 122 and 124.) However, signal lines 122 and 124 are input lines to the multiplexer 118. The multiplexer 118 cannot be the FIFO status providing means and the multiplexer and the read data selection means. Thus, applicants respectfully submit that dependent claims 2-4 are clearly allowable.

Independent method claim 5 is directed to reducing the access times of a FIFO buffer without introducing latency overhead. It recites providing a FIFO, connecting a read data selector to an output of the FIFO and providing simultaneous access to a selected storage location at an odd address and a selected storage location at an even address, providing selection inputs to the read data selector for selecting odd and even read addresses, multiplexing the outputs of the read data selector to enable selection of a desired one of multiple outputs of the read data selector as the final output of the FIFO, and controlling the multiplexer to select one of the read data outputs as a final output of the FIFO and to control selection input to the read data selector for selecting an odd read address and an even read address.

As discussed above with respect to claim 1, nowhere do Rust et al. teach or suggest connecting a read data selector having multiple outputs to the outputs of the FIFO and multiplexing the multiple outputs of the read data selector to enable selection of a desired one of multiple outputs of the read data selector. For this and the other reasons discussed above with respect to claim 1, applicants respectfully submit that claims 5-8 are clearly allowable.

Independent claim 9 is directed to a synchronous FIFO buffer that includes a FIFO circuit, a data select circuit coupled to the FIFO circuit and having first and second data outputs, a multiplexer circuit coupled to the first and second data outputs of the data select circuit, a finite state machine controlling input to the multiplexer circuit and configured to generate control signals to control the output of the multiplexer circuit, and a pointer circuit coupled to a further output of the finite state machine and configured to generate a read address that is output to the data select circuit in response to a further control signal from the finite state machine. Applicants respectfully submit that claim 9 is allowable for the reasons discussed above with respect to claim 1, *i.e.*, that Rust et al. do not teach or suggest the use of a data select circuit between the FIFO circuit and the multiplexer, and Rust et al. do not teach or suggest a finite state machine for controlling the multiplexer circuit. For these reasons as well as for the reasons discussed above with respect to claim 1, applicants respectfully submit that claim 9 and dependent claims 12 and 13 are allowable.

Independent claim 18 is directed to a method for providing access to a FIFO buffer that includes providing simultaneous access to selected storage locations at even and odd addresses from multiple outputs of a FIFO circuit, providing a read data selector having multiple outputs and multiple selection inputs for selecting an odd and even read address, multiplexing an output of the read data selector to enable selection of a desired one of the multiple outputs of the read data selector, and controlling the state of the multiplexer to select one of the multiplexer inputs as the final output of the FIFO and to control the multiple selection inputs to the read data selector for selecting an odd and even read address. Nowhere do Rust et al. teach or suggest providing a read data selector having multiple outputs and multiple selection inputs for selecting an odd and even read address from the FIFO. Moreover, this reference does not teach or suggest controlling the state of a multiplexer to select one of the multiplexer inputs as a final output of the FIFO and to control the multiple selection inputs to the read data selector for selecting an odd read address and an even read address. For these reasons as well as for the reasons discussed above with respect to claim 5, applicants respectfully submit that claims 18-20 are clearly allowable.

Claims 14-17 and claims 10 and 11 were rejected as obvious over Rust et al. in view of Kim et al. The Examiner asserts that Kim et al. teach fetching and assigning words from a FIFO and arranging for "data output not in use (paragraph [0010] and [0011])." Applicants respectfully disagree with this characterization of the teachings of Kim et al.

More particularly, Kim et al. is directed to a first-in, first-out memory system and method having parallel FIFOs with multiple outputs, each of the outputs controlled by a multiplexer assigned to each of the parallel FIFOs. A logic circuit in the form of a flip-flop alternates the simultaneous reading of data. More particularly, as described in paragraph 12, Kim et al. state that a single entry read operation is provided in which a "flip-flop 23 functions as a one-bit read register and the read control signal is used to point to one of FIFO A or FIFO B." Kim et al. states:

> When the read control signal has a logic one value, multiplexer 20 selects the output of FIFO A to provide as an output and multiplexer 22 selects the output of FIFO B to provide as an output. When the read control signal has a logic zero value, multiplexer 20 selects the output of FIFO B to provide as an output and multiplexer 22 selects the output of FIFO A to provide as an output.

In this same paragraph, Kim et al. describe the use of an inverter 24 that "functions to flip the logics data of the flip-flops every time that a single read operation occurs. Additionally, when two read operations occur simultaneously, the logics data flip-flop 23 remains the same."

Thus, Kim et al. utilizes a flip-flop to simultaneously and alternatingly couple the outputs of the two parallel FIFOs to the respective multiplexers for either alternate read or simultaneous read operations. Nowhere does Kim et al. teach or suggest arranging for outputting of data on an output that is not in use.

Claim 14 of the present invention is directed to a FIFO buffer circuit that comprises a FIFO circuit configured to receive, store, and output words to a plurality of outputs, and control means coupled to the FIFO circuit comprising a data select circuit connected to the plurality of FIFO outputs, the data select circuit having first and second data output buses and configured to fetch a next word from the FIFO and assign it to one of the first and second data output buses that is not currently in use. Nowhere do Kim et al. or Rust et al., taken alone or in any combination thereof, teach or suggest such a FIFO buffer circuit. As previously discussed,

Rust et al. do not teach or suggest a data select circuit coupled to the multiple outputs of a FIFO and having first and second data output buses. Kim et al. also fails to teach or suggest such a data select circuit that assigns the output from the FIFO to one of the first and second data output buses that is not currently in use. As discussed above, Kim et al. uses a D flip-flop to assign the outputs of FIFO A and FIFO B to both first and second multiplexers 20, 22 in an alternating fashion. Coupling of the FIFOs to the respective multiplexers is not done on a use-available basis.

Even if one were motivated to combine these two references as the Examiner suggests, the combination would still fall short of the claimed invention. For example, Kim et al. would apply a multiplexer to the output of the even array of Rust et al. and a multiplexer to the odd array of Rust et al. and output these two to an I/O circuit. Nowhere would this combination assign the output of the FIFO to one of the first and second data output buses that is not currently in use. For these reasons, applicants respectfully submit that claim 14, and dependent claims 15 and 16 are clearly allowable.

Independent claim 17 is directed to a method for reducing access time to a FIFO buffer that comprises fetching a next word from a FIFO circuit and assigning it to one of a first data out bus and a second data out bus that is not currently in use. As discussed above with respect to claim 14, nowhere do Rust et al. or Kim et al., taken alone or in combination thereof, teach or suggest such a method. Claims 21 and 22 depend ultimately from claim 17 and recite the use of a data select circuit coupled to an output of the FIFO circuit and a multiplexer coupled to multiple outputs of the data select circuit to assign the next word from the FIFO (claim 21), and using a finite state machine to control a state of the multiplexer and a state of the data select circuit (claim 22). Nowhere do Rust et al. or Kim et al., taken alone or in any combination, teach or suggest these features. Applicants respectfully submit that claim 17 and dependent claims 21 and 22 are clearly allowable.

In view of the foregoing, applicants respectfully submit that all of the claims in this application are in condition for allowance. In the event the Examiner finds minor informalities that can be resolved by telephone conference, the Examiner is urged to contact applicants' undersigned representative by telephone at (206) 622-4900 in order to expeditiously

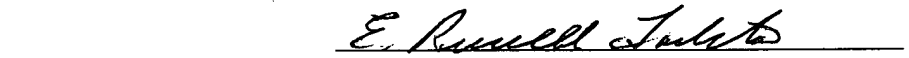
resolve prosecution of this application. Consequently, early and favorable action allowing these claims and passing this case to issuance is respectfully solicited.

The Director is authorized to charge any additional fees due by way of this Amendment, or credit any overpayment, to our Deposit Account No. 19-1090.

All of the claims remaining in the application are now clearly allowable. Favorable consideration and a Notice of Allowance are earnestly solicited.

Respectfully submitted,

SEED Intellectual Property Law Group PLLC



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